

MC14106B

Hex Schmitt Trigger

The MC14106B hex Schmitt Trigger is constructed with MOS P-channel and N-channel enhancement mode devices in a single monolithic structure. These devices find primary use where low power dissipation and/or high noise immunity is desired. The MC14106B may be used in place of the MC14069UB hex inverter for enhanced noise immunity or to “square up” slowly changing waveforms.

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation, V_{in} and V_{out} should be constrained to the range $V_{SS} \leq (V_{in}$ or $V_{out}) \leq V_{DD}$.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}). Unused outputs must be left open.

Features

- Increased Hysteresis Voltage Over the MC14584B
- Supply Voltage Range = 3.0 Vdc to 18 Vdc
- Capable of Driving Two Low-power TTL Loads or One Low-power Schottky TTL Load Over the Rated Temperature Range
- Pin-for-Pin Replacement for CD40106B and MM74C14
- Can Be Used to Replace the MC14584B or MC14069UB
- Pb-Free Packages are Available

MAXIMUM RATINGS (Voltages Referenced to V_{SS})

| Symbol | Parameter | Value | Unit |
|-------------------|---|------------------------|------|
| V_{DD} | DC Supply Voltage Range | -0.5 to +18.0 | V |
| V_{in}, V_{out} | Input or Output Voltage Range (DC or Transient) | -0.5 to $V_{DD} + 0.5$ | V |
| I_{in}, I_{out} | Input or Output Current (DC or Transient) per Pin | ± 10 | mA |
| P_D | Power Dissipation, per Package (Note 1) | 500 | mW |
| T_A | Ambient Temperature Range | -55 to +125 | °C |
| T_{stg} | Storage Temperature Range | -65 to +150 | °C |
| T_L | Lead Temperature (8-Second Soldering) | 260 | °C |

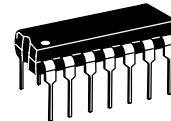
Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

1. Temperature Derating: Plastic “P and D/DW” Packages: - 7.0 mW/°C From 65°C To 125°C



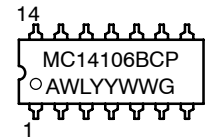
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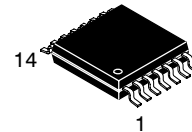
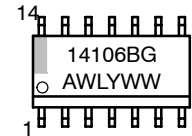


PDIP-14
P SUFFIX
CASE 646

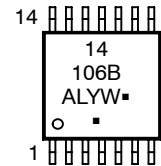
MARKING DIAGRAMS



SOIC-14
D SUFFIX
CASE 751A



TSSOP-14
DT SUFFIX
CASE 948G



A = Assembly Location
WL, L = Wafer Lot
YY, Y = Year
WW, W = Work Week
G or ■ = Pb-Free Package

(Note: Microdot may be in either location)

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 2 of this data sheet.

MC14106B

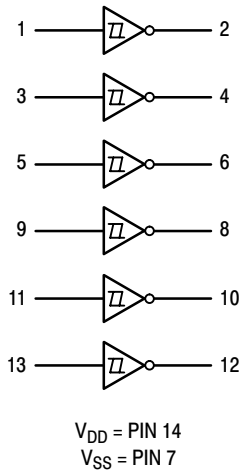


Figure 1. Logic Diagram

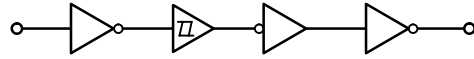


Figure 2. Equivalent Circuit Schematic
(1/6 of Circuit Shown)

ORDERING INFORMATION

| Device | Package | Shipping [†] |
|---------------|----------------------|-----------------------|
| MC14106BCP | PDIP-14 | 25 Units / Rail |
| MC14106BCPG | PDIP-14 (Pb-Free) | |
| MC14106BD | SOIC-14 | 55 Units / Rail |
| MC14106BDG | SOIC-14 (Pb-Free) | |
| MC14106BDR2 | SOIC-14 | 2500 / Tape & Reel |
| MC14106BDR2G | SOIC-14 (Pb-Free) | |
| MC14106BDTR2 | TSSOP-14* | |
| MC14106BDTR2G | TSSOP-14* | |

[†]For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

*This package is inherently Pb-Free.

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ELECTRICAL CHARACTERISTICS (Voltages Referenced to V_{SS})

| Characteristic | Symbol | V_{DD} Vdc | - 55°C | | 25°C | | | 125°C | | Unit | |
|---|---------------------------|-----------------|--|-----------|-------|--------------------|-----------|-------|-----------|-----------------|------|
| | | | Min | Max | Min | Typ ⁽²⁾ | Max | Min | Max | | |
| Output Voltage $V_{in} = V_{DD}$ $V_{in} = 0$ | "0" Level V_{OL} | 5.0 | - | 0.05 | - | 0 | 0.05 | - | 0.05 | Vdc | |
| | | 10 | - | 0.05 | - | 0 | 0.05 | - | 0.05 | | |
| | | 15 | - | 0.05 | - | 0 | 0.05 | - | 0.05 | | |
| | "1" Level V_{OH} | 5.0 | 4.95 | - | 4.95 | 5.0 | - | 4.95 | - | | Vdc |
| | | 10 | 9.95 | - | 9.95 | 10 | - | 9.95 | - | | |
| | | 15 | 14.95 | - | 14.95 | 15 | - | 14.95 | - | | |
| Hysteresis Voltage | V_H ⁽⁵⁾ | 5.0 | 0.3 | 2.0 | 0.3 | 1.1 | 2.0 | 0.3 | 2.0 | Vdc | |
| | | 10 | 1.2 | 3.4 | 1.2 | 1.7 | 3.4 | 1.2 | 3.4 | | |
| | | 15 | 1.6 | 5.0 | 1.6 | 2.1 | 5.0 | 1.6 | 5.0 | | |
| Threshold Voltage Positive-Going Negative-Going | V_{T+} | 5.0 | 2.2 | 3.6 | 2.2 | 2.9 | 3.6 | 2.2 | 3.6 | Vdc | |
| | | 10 | 4.6 | 7.1 | 4.6 | 5.9 | 7.1 | 4.6 | 7.1 | | |
| | | 15 | 6.8 | 10.8 | 6.8 | 8.8 | 10.8 | 6.8 | 10.8 | | |
| | V_{T-} | 5.0 | 0.9 | 2.8 | 0.9 | 1.9 | 2.8 | 0.9 | 2.8 | | Vdc |
| | | 10 | 2.5 | 5.2 | 2.5 | 3.9 | 5.2 | 2.5 | 5.2 | | |
| | | 15 | 4.0 | 7.4 | 4.0 | 5.8 | 7.4 | 4.0 | 7.4 | | |
| Output Drive Current $(V_{OH} = 2.5 \text{ Vdc})$ $(V_{OH} = 4.6 \text{ Vdc})$ $(V_{OH} = 9.5 \text{ Vdc})$ $(V_{OH} = 13.5 \text{ Vdc})$ $(V_{OL} = 0.4 \text{ Vdc})$ $(V_{OL} = 0.5 \text{ Vdc})$ $(V_{OL} = 1.5 \text{ Vdc})$ | Source I_{OH} | 5.0 | -3.0 | - | -2.4 | -4.2 | - | -1.7 | - | mAdc | |
| | | 5.0 | -0.64 | - | -0.51 | -0.88 | - | -0.36 | - | | |
| | | 10 | -1.6 | - | -1.3 | -2.25 | - | -0.9 | - | | |
| | | 15 | -4.2 | - | -3.4 | -8.8 | - | -2.4 | - | | |
| | Sink I_{OL} | 5.0 | 0.64 | - | 0.51 | 0.88 | - | 0.36 | - | | mAdc |
| | | 10 | 1.6 | - | 1.3 | 2.25 | - | 0.9 | - | | |
| 15 | | 4.2 | - | 3.4 | 8.8 | - | 2.4 | - | | | |
| Input Current | I_{in} | 15 | - | ± 0.1 | - | ± 0.00001 | ± 0.1 | - | ± 1.0 | μAdc | |
| Input Capacitance $(V_{in} = 0)$ | C_{in} | - | - | - | - | 5.0 | 7.5 | - | - | pF | |
| Quiescent Current (Per Package) | I_{DD} | 5.0 | - | 0.25 | - | 0.0005 | 0.25 | - | 7.5 | μAdc | |
| | | 10 | - | 0.5 | - | 0.0010 | 0.5 | - | 15 | | |
| | | 15 | - | 1.0 | - | 0.0015 | 1.0 | - | 30 | | |
| Total Supply Current (Note 3, 4) (Dynamic plus Quiescent, Per Package) $(C_L = 50 \text{ pF}$ on all outputs, all buffers switching) | I_T | 5.0 10 15 | $I_T = (1.8 \mu\text{A/kHz}) f + I_{DD}$ $I_T = (3.6 \mu\text{A/kHz}) f + I_{DD}$ $I_T = (5.4 \mu\text{A/kHz}) f + I_{DD}$ | | | | | | | μAdc | |

2. Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.

3. The formulas given are for the typical characteristics only at 25°C.

4. To calculate total supply current at loads other than 50 pF:

$$I_T(C_L) = I_T(50 \text{ pF}) + (C_L - 50) \text{ Vfk where } I_T \text{ is in } \mu\text{A (per package)}, C_L \text{ in pF, } V = (V_{DD} - V_{SS}) \text{ in volts, } f \text{ in kHz is input frequency, and } k = 0.001.$$

5. $V_H = V_{T+} - V_{T-}$ (But maximum variation of V_H is specified as less than $V_{T+ \text{ max}} - V_{T- \text{ min}}$).

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SWITCHING CHARACTERISTICS ($C_L = 50 \text{ pF}$, $T_A = 25^\circ\text{C}$)

| Characteristic | Symbol | V_{DD} Vdc | Min | Typ (6) | Max | Unit |
|------------------------|-----------------------|-----------------|-----|---------|-----|------|
| Output Rise Time | t_{TLH} | 5.0 | – | 100 | 200 | ns |
| | | 10 | – | 50 | 100 | |
| | | 15 | – | 40 | 80 | |
| Output Fall Time | t_{THL} | 5.0 | – | 100 | 200 | ns |
| | | 10 | – | 50 | 100 | |
| | | 15 | – | 40 | 80 | |
| Propagation Delay Time | t_{PLH} , t_{PHL} | 5.0 | – | 125 | 250 | ns |
| | | 10 | – | 50 | 100 | |
| | | 15 | – | 40 | 80 | |

6. Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.

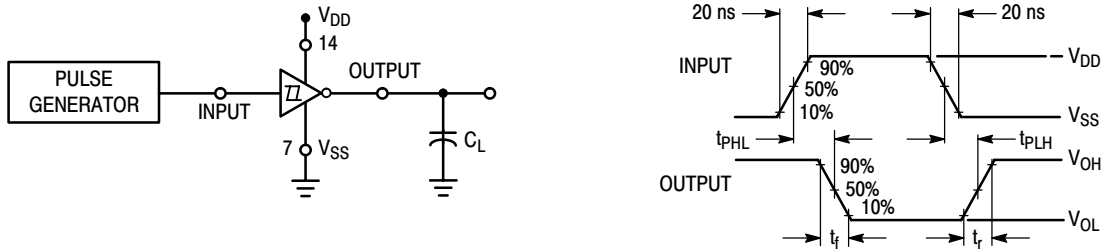


Figure 1. Switching Time Test Circuit and Waveforms

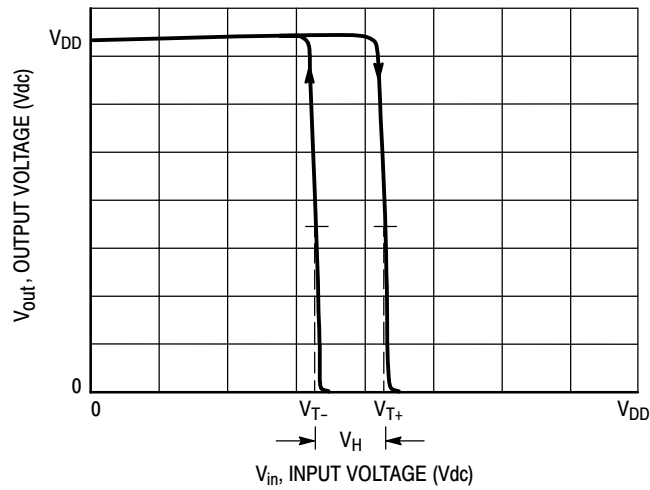


Figure 2. Typical Transfer Characteristics

MC14106B

APPLICATIONS

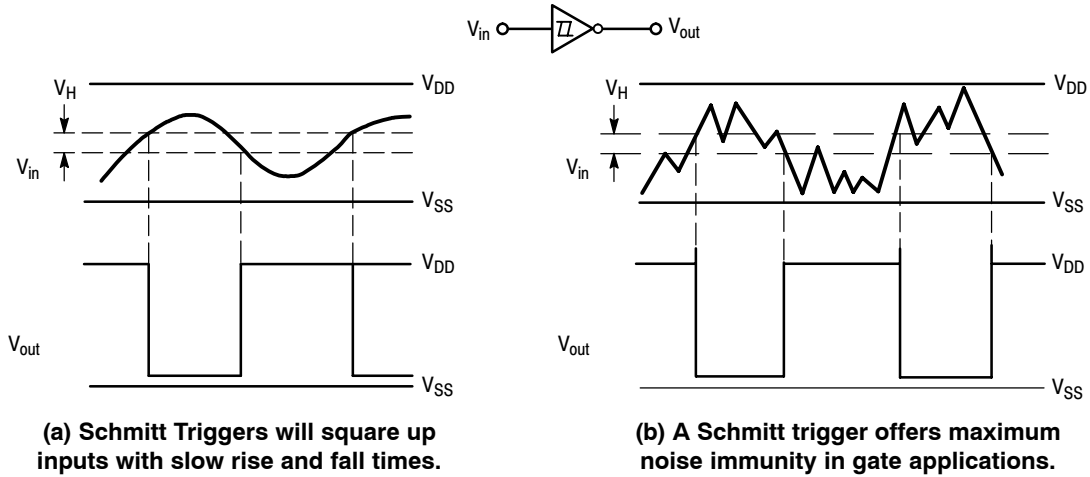
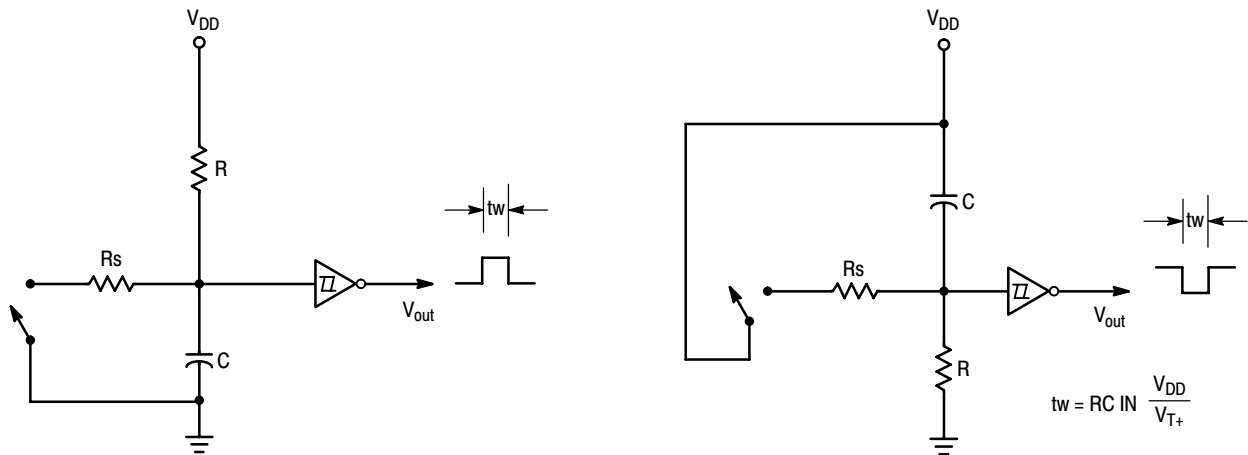


Figure 3.



Useful as Pushbutton/Keyboard Debounce Circuit.

Figure 4. Monostable Multivibrator

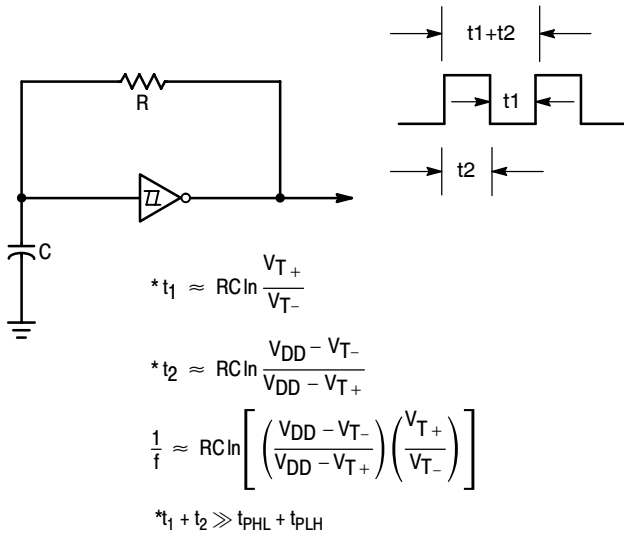


Figure 5. Astable Multivibrator

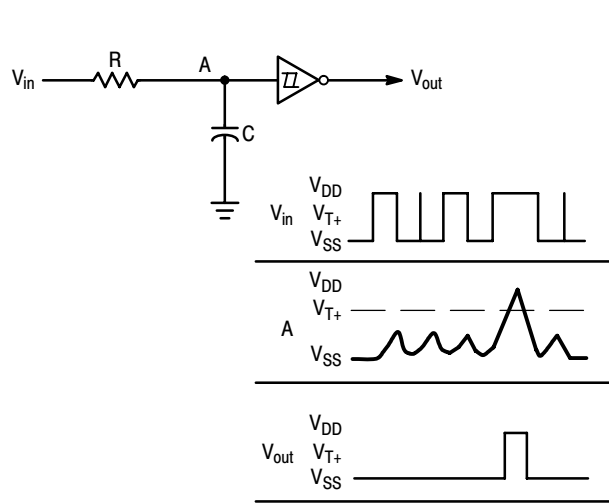
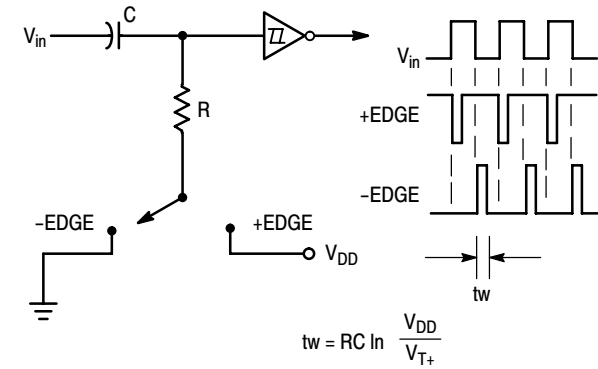


Figure 6. Integrator



Useful as an edge detector circuit.

Figure 7. Differentiator

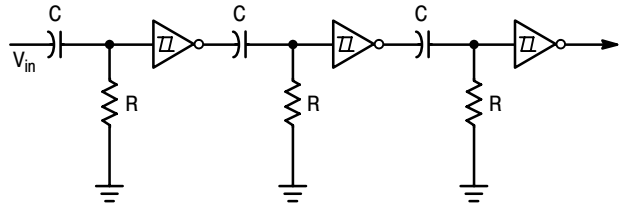
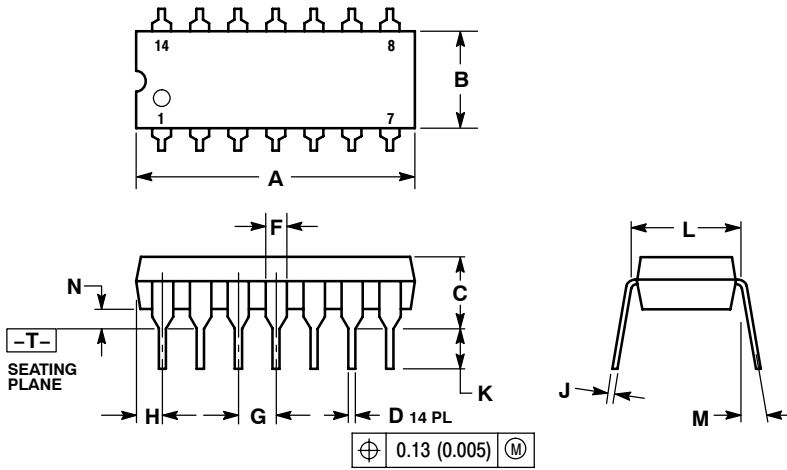


Figure 8. Positive Edge Time Delay Circuit

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PACKAGE DIMENSIONS

PDIP-14
CASE 646-06
ISSUE P



NOTES:

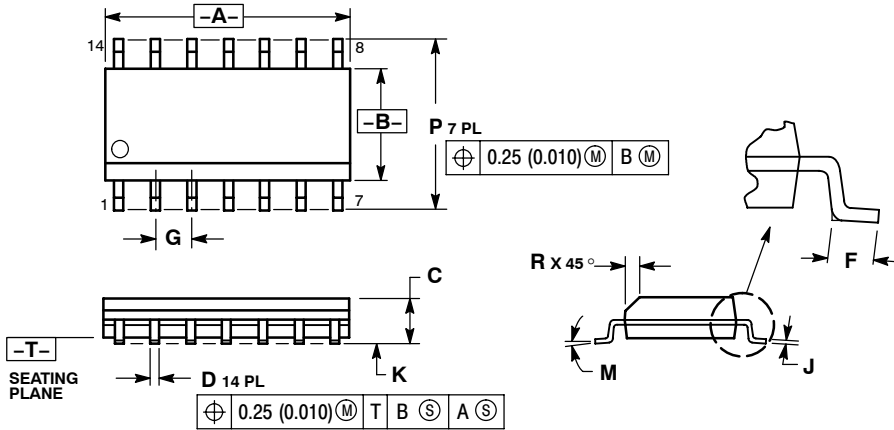
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSION L TO CENTER OF LEADS WHEN FORMED PARALLEL.
4. DIMENSION B DOES NOT INCLUDE MOLD FLASH.
5. ROUNDED CORNERS OPTIONAL.

| DIM | INCHES | | MILLIMETERS | |
|-----|-----------|-------|-------------|-------|
| | MIN | MAX | MIN | MAX |
| A | 0.715 | 0.770 | 18.16 | 19.56 |
| B | 0.240 | 0.260 | 6.10 | 6.60 |
| C | 0.145 | 0.185 | 3.69 | 4.69 |
| D | 0.015 | 0.021 | 0.38 | 0.53 |
| F | 0.040 | 0.070 | 1.02 | 1.78 |
| G | 0.100 BSC | | 2.54 BSC | |
| H | 0.052 | 0.095 | 1.32 | 2.41 |
| J | 0.008 | 0.015 | 0.20 | 0.38 |
| K | 0.115 | 0.135 | 2.92 | 3.43 |
| L | 0.290 | 0.310 | 7.37 | 7.87 |
| M | --- | 10° | --- | 10° |
| N | 0.015 | 0.039 | 0.38 | 1.01 |

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PACKAGE DIMENSIONS

SOIC-14
CASE 751A-03
ISSUE H

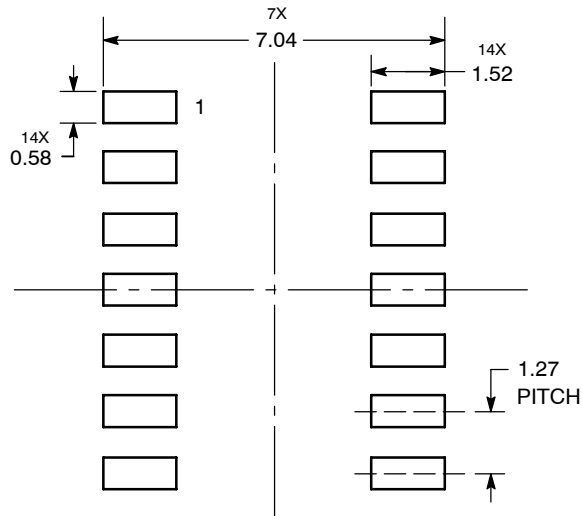


NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.

| MILLIMETERS | | INCHES | | |
|-------------|----------|--------|-----------|-------|
| DIM | MIN | MAX | MIN | MAX |
| A | 8.55 | 8.75 | 0.337 | 0.344 |
| B | 3.80 | 4.00 | 0.150 | 0.157 |
| C | 1.35 | 1.75 | 0.054 | 0.068 |
| D | 0.35 | 0.49 | 0.014 | 0.019 |
| F | 0.40 | 1.25 | 0.016 | 0.049 |
| G | 1.27 BSC | | 0.050 BSC | |
| J | 0.19 | 0.25 | 0.008 | 0.009 |
| K | 0.10 | 0.25 | 0.004 | 0.009 |
| M | 0° | 7° | 0° | 7° |
| P | 5.80 | 6.20 | 0.228 | 0.244 |
| R | 0.25 | 0.50 | 0.010 | 0.019 |

SOLDERING FOOTPRINT*



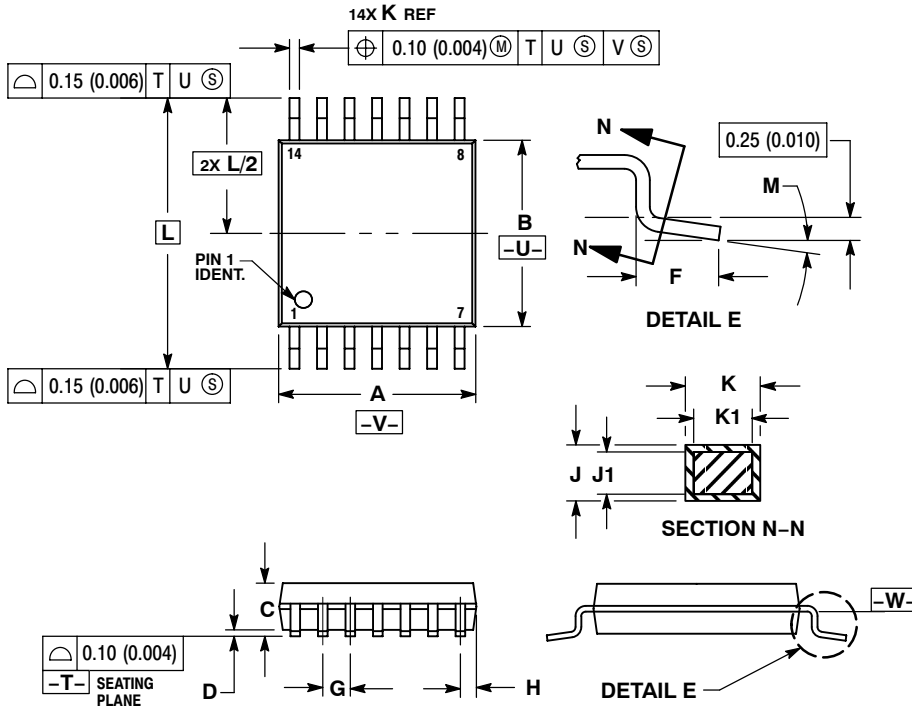
DIMENSIONS: MILLIMETERS

*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

MC14106B

PACKAGE DIMENSIONS

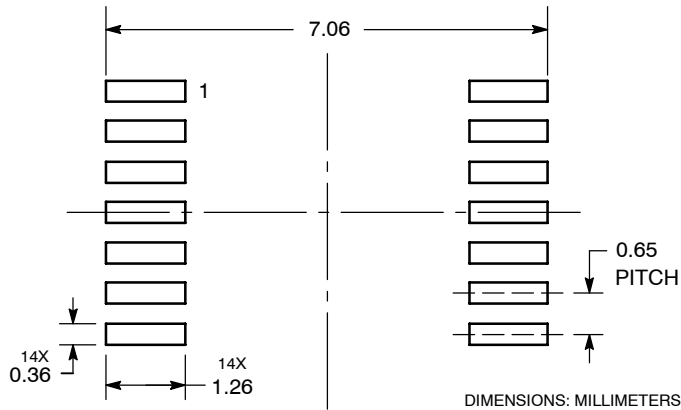
TSSOP-14
CASE 948G-01
ISSUE B



- NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
 2. CONTROLLING DIMENSION: MILLIMETER.
 3. DIMENSION A DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
 4. DIMENSION B DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 (0.010) PER SIDE.
 5. DIMENSION K DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE K DIMENSION AT MAXIMUM MATERIAL CONDITION.
 6. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
 7. DIMENSION A AND B ARE TO BE DETERMINED AT DATUM PLANE -W-

| DIM | MILLIMETERS | | INCHES | |
|-----|-------------|------|-----------|-------|
| | MIN | MAX | MIN | MAX |
| A | 4.90 | 5.10 | 0.193 | 0.200 |
| B | 4.30 | 4.50 | 0.169 | 0.177 |
| C | --- | 1.20 | --- | 0.047 |
| D | 0.05 | 0.15 | 0.002 | 0.006 |
| F | 0.50 | 0.75 | 0.020 | 0.030 |
| G | 0.65 BSC | | 0.026 BSC | |
| H | 0.50 | 0.60 | 0.020 | 0.024 |
| J | 0.09 | 0.20 | 0.004 | 0.008 |
| J1 | 0.09 | 0.16 | 0.004 | 0.006 |
| K | 0.19 | 0.30 | 0.007 | 0.012 |
| K1 | 0.19 | 0.25 | 0.007 | 0.010 |
| L | 6.40 BSC | | 0.252 BSC | |
| M | 0° 8° | | 0° 8° | |

SOLDERING FOOTPRINT*



*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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